

### **REMARKS**

In response to the Office Action mailed March 14, 2007, Applicant respectfully requests reconsideration. Claims 1-85 were previously pending in this application. Applicant elected to pursue claims 1-70 in this application by way of the Response to the Restriction Requirement mailed December 19, 2006. Non-elected claims 71-85 are canceled herein along with previously pending claims 6, 21, 37, 57 and 58. In addition, claims 1, 7, 16, 22, 31, 38, 51 and 59-62 are amended. No claims are added. As a result, claims 1-5, 7-20, 22-36, 38-56 and 59-70 are pending for examination with claims 1, 16, 31 and 51 being independent.

#### **I. Rejections Under 35 U.S.C. §112**

The Office Action rejects claims 1-30 under 35 U.S.C. 112, second paragraph, as purportedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office Action asserts that the term “the first state vector” in claims 1 and 16 lacks antecedent basis. Claims 1 and 16 have been amended to replace the term “the first state vector” with the term “the initial state vector,” which has antecedent basis in the respective claims. Accordingly, Applicant respectfully requests that the rejection of claims 1-30 under 35 U.S.C. 112, second paragraph, be withdrawn.

#### **II. Rejections Under 35 U.S.C. §101**

The Office Action rejects claims 1-70 under 35 U.S.C. §101 as purportedly being directed to non-statutory subject matter. Applicant respectfully disagrees. The Office Action asserts that the “the claimed invention must transform an article or physical object to a different state or thing, or produce a useful, concrete and tangible result,” citing *State Street Bank & Trust Co. v. Signature Financial Group, Inc.* 149 F.3d 1368 as the authority. However, this assertion is only partially correct. The standard articulated by the court in *State Street* is that the claimed invention must produce a useful, concrete and tangible result. Transforming an article or physical object to a different state or thing is not part of the analysis in determining whether a mathematical algorithm is statutory subject matter under §101.

Thus, the fact that a claim “merely involves calculations and manipulations of data in performing computations,” and that the “inputs are numbers and output are also numbers,” as

indicated in the Office Action is not relevant to this analysis. In fact, *State Street* is very clear on this point, stating that “the mere fact that a claimed invention involves inputting numbers, calculating numbers, outputting numbers, and storing numbers, in and of itself, would not render it non-statutory subject matter, unless, of course *its operation does not produce a “useful, concrete and tangible result,”* *Id.* at 1374 (emphasis added). Accordingly, the claims should be analyzed only under the useful, concrete and tangible result standard.

While Applicant believes that the claims, as previously presented, produce a useful, concrete and tangible result, Applicant has amended the claims to address the Examiner’s concern with respect to §101. The claims are not amended for reasons related to patentability. Each of the independent claims have been amended to recite that the offset sequence is generated for use as a pseudo-random number (PN) code for a wireless communication. PN codes may be used to modulate signals in code division multiple access (CDMA) wireless communications, for example, and therefore generation of such sequences produces a useful, concrete and tangible result. Accordingly, Applicant respectfully requests that the rejections under 35 U.S.C. §101 be withdrawn.

### **III. Rejections Under 35 U.S.C. §102**

The Office Action rejects claims 1-2, 5, 16-18, 20, 31-34, 36, 47 and 51-56 under 35 U.S.C. 102(b) as purportedly being anticipated by US Patent No. 6,295,301 (Asano). While Applicant believes the claims, as previously presented, distinguish over Asano, Applicant has amended the claims to further the prosecution of this application.

Initially, Applicant points out that the Office Action does not reject claims 4, 6-15, 19, 21-30, 35, 37-46 and 57-66 under either 35 U.S.C. §§102 or 103 in the body of the Office Action. By this amendment, each of the independent claims have been amended to incorporate subject matter of one or more of the claims that were not rejected by the Office Action based on prior art. In particular, claim 1 is amended to incorporate subject matter recited in previously pending claim 6. Claim 16 has been amended to incorporate subject matter recited in previously pending claim 21. Claim 31 has been amended to incorporate subject matter recited in previously pending claim 37, and claim 51 has been amended to incorporate subject matter recited in previously pending claims 57 and 58.

While Applicant does not agree that Asano anticipates the claims as previously presented, the claims as amended include additional subject matter that is not disclosed or suggested by Asano. In particular, Asano does not disclose or suggest generating a plurality of bits of an offset sequence on each successive iteration. Asano discloses determining an advanced state of a PN code generator resulting from a stop interval (e.g., a power down period) such that when the PN code generator is restarted, the PN code generator obtains the same state as if it had been operating continuously through the stop interval (col. 2, lines 13-33). However, Asano does not discuss how the PN code generator operates after the advanced state has been obtained, except in col. 8, lines 42-46, which state:

When the state of PN code generating section reaches the state after shifted the specific times (i), shift clock 104 is inputted at the desired timing corresponding to the number of shift times (i), and the generation of PN code is initiated in PN code generating section 100. (Emphasis added).

It should be appreciated that PN code generating section 100 is a conventional feedback shift register, which generates bits of a PN code one bit on each iteration, e.g., one bit on each clocked shift of the shift register (see FIG. 7 and col. 5, line 33-col. 6, line 26). Asano is directed to methods of computing an advanced state to initialize a PN code generator to begin generating a PN code. The only disclosure related to how the PN code generator actually generates the PN code is in the context of a conventional shift register, which generates one bit at a time on each successive shift of the shift register. Asano is completely silent with respect to generating a plurality of bits on each iteration. Accordingly, the claims patentably distinguish over Asano, as discussed in further detail below in connection with each of the claims.

A. Claims 1-5 and 7-15

Nowhere does Asano disclose or suggest a method of generating an offset sequence “wherein generating the offset sequence includes generating a plurality of bits of the offset sequence on each of a plurality of iterations, each of the plurality of iterations comprising acts of providing i bits of the current state vector as a first portion of the offset sequence, i having a value greater than 1, and computing a subsequent state vector advanced at least i states from the current state vector, the subsequent state vector operating as the current state vector for a next

iteration,” as recited in claim 1. Therefore, claim 1 patentably distinguishes over Asano and is in allowable condition. Claims 2-5 and 7-15 depend from claim 1 and are allowable based at least on their dependency.

B. Claims 16-20 and 22-30

Nowhere does Asano disclose or suggest a computer readable medium encoded with instructions for execution on at least one processor, the instructions, when executed on the at least one processor, generates an offset sequence “wherein generating the offset sequence includes generating a plurality of bits of the offset sequence on each of a plurality of iterations, each of the plurality of iterations comprising acts of providing  $i$  bits of the current state vector as a first portion of the offset sequence,  $i$  having a value greater than 1, and computing a subsequent state vector advanced at least  $i$  states from the current state vector, the subsequent state vector operating as the current state vector for a next iteration,” as recited in claim 16. Therefore, claim 16 patentably distinguishes over Asano and is in allowable condition. Claims 17-20 and 22-30 depend from claim 16 and are allowable based at least on their dependency.

C. Claims 31-36 and 38-50

Nowhere does Asano disclose or suggest a computer readable medium encoded with instructions for execution on at least one processor, the instructions, when executed on the at least one processor, generates an offset sequence “wherein a plurality of bits of the offset sequence are generated on each of a plurality of iterations, each of the plurality of iterations including providing  $i$  bits of the current state of the sequence generator as a first portion of the offset sequence,  $i$  having a value greater than 1, and computing a next state of the sequence generator advanced at least  $i$  states from the current state, the next state operating as the current state of the sequence generator on a next iteration,” as recited in claim 31. Therefore, claim 31 patentably distinguishes over Asano and is in allowable condition. Claims 32-36 and 38-50 depend from claim 31 and are allowable based at least on their dependency.

D. Claims 51-56 and 59-70

Nowhere does Asano disclose or suggest a sequence generator having a first component and a second component “wherein the first component is adapted to simultaneously provide at least two bits of the current state associated with the reference sequence as a portion of the offset sequence on each of a plurality of iterations of the sequence generator, and wherein the second

component is further adapted to compute a next state advanced from the current state by at least two of the plurality of states on each of the plurality of iterations, the next state operating as the current state in a next iteration,” as recited in claim 51. Therefore, claim 51 patentably distinguishes over Asano and is in allowable condition. Claims 52-56 and 59-60 depend from claim 51 and are allowable based at least upon their dependency.

**CONCLUSION**

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,  
*Wei An, Applicant*

By: *William R. McClellan*  
William R. McClellan, Reg. No. 29,409  
Wolf, Greenfield & Sacks, P.C.  
600 Atlantic Avenue  
Boston, Massachusetts 02210-2206  
Telephone: (617) 646-8000

Docket No.: A0312.70495US00  
Date: September 13, 2007  
x9/14/07x